U.S. Serial No. 09/301,284

AMENDMENT TO THE CLAIMS

1. (Canceled)

2. (Currently amended) The processor of Claim 49, including a first ~~program counter~~ address indicator updating means and a second ~~program counter~~ address indicator updating means,

the second ~~program counter~~ address indicator updating means incrementing a value of the second ~~program counter~~ address indicator in accordance with an amount of instructions that were executed in a preceding cycle and sending any carry generated in an incrementing to the first ~~program counter~~ address indicator updating means, and

the first ~~program counter~~ address indicator updating means adding the carry received from the second ~~program counter~~ address indicator updating means to the value of the first ~~program counter~~ address indicator.

3. (Currently amended) The processor of Claim 2, further including:

program counter relative value extracting means for extracting, when an instruction being executed includes a program counter relative value that is based on an address of a first instruction executed in a present cycle, the program counter relative value; and

calculating means for adding the program counter relative value to the value of the first ~~program counter~~ address indicator and the value of the second ~~program counter~~ address indicator, and setting an addition result as the value of the first ~~program counter~~ address indicator and the value of the second ~~program counter~~ address indicator.

4. (Currently amended) The processor of Claim 3, wherein the calculating means includes a first calculating unit and a second calculating unit,

the second calculating unit adding the value of the second ~~program counter~~ address indicator and lower bits of the program counter relative value, setting a result of an addition as the value of the second ~~program counter~~ address indicator, and sending any carry generated in the addition to the first calculating unit,

the first calculating unit adding the value of the first ~~program counter~~ address indicator, upper bits of the program counter relative value, and any carry received from the second calculating unit, and setting a result of an addition as the value of the first ~~program counter~~ address indicator.

5. (Currently amended) The processor of Claim 3, wherein the calculating means includes a first calculating unit and a second calculating unit,

the second calculating unit adding the value of the second ~~program counter~~ address indicator and lower bits of the program counter relative value without generating a carry, and setting a result of an addition as the value of the second ~~program counter~~ address indicator,

the first calculating unit adding the value of the first ~~program counter~~ address indicator and upper bits of the program counter relative value, and setting a result of an addition as the value of the first program counter.

6. (Currently amended) The program counter of Claim 3, wherein the calculating means adds the value of the first ~~program counter~~ address indicator and upper bits of the program

counter relative value, sets a result of an addition as the value of the first ~~program counter~~ address indicator, and sets lower bits of the program counter relative value as the value of the second ~~program counter~~ address indicator.

7. (Currently amended) The processor of Claim 3, wherein the calculating means adds the program counter relative value and a value whose upper bits are the value of the first ~~program counter~~ address indicator and lower bits are the value of the second ~~program counter~~ address indicator, and sets upper bits of a result of an addition as the value of the first ~~program counter~~ address indicator and lower bits of the result as the second ~~program counter~~ address indicator.

8. (Currently amended) The processor of Claim 2, further including:

program counter relative value extracting means for extracting, when an executed instruction includes a program counter relative value that is based on an address of the executed instruction, the program counter relative value;

program counter amending means for amending the value of the first ~~program counter~~ address indicator and the value of the second ~~program counter~~ address indicator to indicate an address of the executed instruction; and

calculating means for adding the program counter relative value, the value of the first ~~program counter~~ address indicator, and the value of the second ~~program counter~~ address indicator, and setting a result of an addition as the value of the first ~~program counter~~ address indicator and the value of the second ~~program counter~~ address indicator.

9. (Currently amended) The processor of Claim 2, further including:

program counter relative value calculating instruction decoding means for decoding a program counter relative value calculating instruction that performs an addition using a program counter relative value and one of

(a) a value of the program counter stored in a register, and

(b) the value of the first ~~program counter~~ address indicator and the value of the second ~~program counter~~ address indicator;

calculating means for performing the addition indicated by the program counter relative value calculating instruction to generate an addition result; and

program counter value updating means for storing the addition result in one of

(a) the register, and

(b) the first ~~program counter~~ address indicator and the second ~~program counter~~ address indicator.

10. (Currently amended) The processor of Claim 49, wherein the first ~~program counter~~ address indicator indicates bits of a memory address more significant than a $1 + log_2 n^{th}$ bit from a least significant, the memory address specifying the storage position of the processing packet in memory, and n being a length of a processing packet in bytes.

11. (Previously presented) The processor of Claim 10, further including

an instruction buffer for temporarily storing instructions; and

instruction reading means for transferring instructions being made of an integer number of bytes from the memory to the instruction buffer, in accordanc with available space in the

instruction buffer but regardless of a size of a processing packet.

12-48. (Canceled)

49. (Currently amended) A processor for reading instructions from a memory ~~according to a program counter, and for executing the read instruction,~~ comprising:

~~the~~ a memory ~~storing~~ configured to store, in a position corresponding to a byte boundary, at least one processing packet being made of a natural number of bytes, the processing packet including processing target instructions, each processing target instruction being an operation to be executed by the processor, the number of processing target instructions being any natural number except for a power of 2[[,]];

~~the program counter including a first program counter and a second program counter,~~

~~the~~ a first address indicator ~~program counter~~ ~~indicating~~ configured to indicate a storage position of the processing packet in the memory[[,]]; and

~~the~~ a second address indicator ~~program counter~~ ~~indicating~~ configured to indicate a position of a processing target instruction in the processing packet by using the same number of ~~values~~ positions as the number of processing target instructions, and cycling through the ~~values~~ positions, ~~and sending a carry to the first program counter if~~

wherein after the second ~~program counter~~ address indicator finished ~~cycles~~ cycling through the positions, the first address indicator indicates the next storage position of the processing packet in the memory.

50. (Currently Amended) A processor system for reading and executing a plurality of target instructions, comprising:

a memory for storing a packet which includes the plurality of target instructions where each of the plurality of target instructions is an operation executable by the processor, the number of the plurality of target instructions is equal to m where m is a natural number other than a number equal to 2^n, where n is a positive integer greater than or equal to 1;

a first ~~program counter~~ address indicator, operably coupled to the memory, for identifying the location of the packet in the memory; and

a second ~~program counter~~ address indicator, operably coupled to the memory, for identifying the location of each of the plurality of instructions in the packet by using the number of the plurality of target instructions to proceed to a preceding or subsequent target instruction.

51. (Currently amended) A processor for reading instructions from a memory according to a program counter, and for executing the read instruction[[,]] comprising:

~~the~~ a memory ~~storing~~ configured to store, in a position corresponding to a byte boundary, at least one processing packet being made of a natural number of bytes, the processing packet including processing target instructions, each processing target instruction being an operation to be executed by the processor, the number of processing target instructions being any natural number except for a power of 2[[,]];

~~the program counter including a first program counter and a second program counter,~~

~~the~~ a first ~~program counter~~ address indicator ~~indicating~~ configured to indicate a storage position of the processing packet in the memory[[,]]; and

~~the~~ a second ~~program counter~~ address indicator ~~indicating~~ configured to indicate a position of processing target instruction in the processing packet, ~~and sending a carry to the first program counter~~

wherein after the second indicator finished indicating every processing target instruction in the packet, the first address indicator indicates the next storage position of the processing packet in the memory.